I CLAIM:

1. An apparatus, comprising:

a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an output that is coupled to a common node, an input that is arranged to receive a feedback signal, and a null control input that is arranged to receive a respective null control signal;

a second stage circuit that is arranged to provide a reference signal to an output node in response to an intermediate signal that is associated with the common node;

a feedback circuit that is arranged to provide the feedback signal in response to the reference signal; and

a null control logic circuit that is arranged to provide a set of null control signals, where each null control signal is associated with a respective one of the amplifiers such that the amplifiers are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.

2. The apparatus of Claim 1, wherein each of the amplifier circuits in the first stage circuit includes a differential pair circuit, wherein each differential pair circuit comprises at least one of: an n-type transistor pair, a p-type transistor pair, a FET type transistor pair, and a BJT type transistor pair.

3. The apparatus of Claim 1, wherein at least one of the amplifier circuits includes a trans-conductance cell, wherein the trans-conductance cell comprises: a differential pair circuit that is coupled to a current mirror circuit, wherein the differential pair circuit is arranged to: receive a differential signal from a first node and a second node, and provide at least a portion of the intermediate signal to the common node in response to the differential signal.

4. The apparatus of Claim 1, wherein at least one of the amplifier circuits includes a switching circuit that is arranged to selectively zero the offset voltage

associated with the trans-conductance cell in response to a selected one of the null control signals.

5. The apparatus of Claim 1, wherein at least one of the amplifier circuits comprises:

a trans-conductance cell, wherein the trans-conductance cell comprises: a differential pair circuit that is coupled to a current mirror circuit, wherein the differential pair circuit is arranged to: receive a differential signal from a first node and a second node, and provide at least a portion of the intermediate signal to the common node in response to the differential signal; and

a switching circuit that is arranged to selectively zero the offset voltage associated with the trans-conductance cell in response to a selected null control signals.

6. The apparatus of Claim 5, wherein the switching circuit is further arranged to selectively couple the differential signal across the first node and the second node when the selected null control signal is deasserted.

7. The apparatus of Claim 5, wherein the switching circuit is further arranged to selectively couple the first and second nodes together when the selected null control signal is asserted.

8. The apparatus of Claim 5, wherein the switching circuit is further arranged to selectively couple the differential signal across the first node and the second node when the selected null control signal is deasserted, and also arranged to selectively couple the first and second nodes together when another selected null control signal is asserted.

9. The apparatus of Claim 8, wherein the switching circuit is further arranged to: selectively couple a first capacitor to the third node when the other null control signal is asserted, and selectively couple a second capacitor to the common node when the other null control signal is asserted.

10. The apparatus of Claim 1, wherein at least one of the amplifier circuits includes a trans-conductance cell that comprises:

a first transistor that includes a source that is coupled to a seventh node, a gate that is coupled to the first node, and a drain that is coupled to a third node;

a second transistor that includes a source that is coupled to the seventh node, a gate that is coupled to the second node, and a drain that is coupled to the common node;

a third transistor that includes a source that is coupled to a power supply node, a gate hat is coupled to the third node, and a drain that is coupled to the common node;

a fourth transistor that includes a source that is coupled to the power supply node, and a gate and drain that are coupled to the third node; and

a fifth transistor that is arranged to operate as a current source that is coupled to the seventh node.

11. The apparatus of Claim 10, further comprising:

a sixth transistor that include a source that is coupled to the power supply node, a gate that is coupled to a sixth node, and a drain that is coupled to the common node;

a seventh transistor that include a source that is coupled to the power supply node, a gate that is coupled to a fifth node, and a drain that is coupled to the third node;

a first capacitor that is coupled between the fifth node and the power supply node;

a second capacitor that is coupled between the sixth node and the power supply node;

a fourth switching transistor that is arranged to selectively couple the fifth node to the third node when actuated; and

a fifth switching transistor that is arranged to selectively couple the sixth node to the common node when actuated.

12. The apparatus of Claim 11, further comprising.

a first switching transistor that is arranged to couple the feedback signal to the first node when actuated;

a second switching transistor that is arranged to couple a reference signal to the second node when actuated; and

a third switching transistor that is arranged to couple the first node to the second node when actuated.

13. The apparatus of Claim 1, wherein the first stage circuit, the second stage circuit, the feedback circuit, and the feedback circuit are configured to operate as at least one of: a switching regulator circuit, a reference voltage circuit, a low drop out (LDO) regulator circuit, and a band-gap reference circuit.

14. The apparatus of Claim 1, wherein the feedback circuit includes a band-gap core circuit, wherein the band-gap core circuit comprises: a first transistor that is coupled between a power supply node and an eight node, a second transistor that is coupled between the power supply node and a ninth node, a first resistor that is coupled between the eighth node and a tenth node, a second resistor that is coupled between the tenth node and the output node, and a third resistor that is coupled between the ninth node and the output node, wherein the feedback signal is associated with at least one of the ninth node and the tenth node.

15. An apparatus, comprising:

a first amplifier means that includes a first output that is coupled to a common node, a first input that is arranged to receive a feedback signal, and a first null control input that is arranged to receive a first null control signal;

a second amplifier means that includes a second output that is coupled to the common node, a second input that is arranged to receive the feedback signal, and a second null control input that is arranged to receive a second null control signal;

a second stage means that is arranged to provide a reference signal in response to an intermediate signal, wherein the intermediate signal is associated with the common node;

a feedback means that is arranged to provide the feedback signal in response to the reference signal; and

a null control means that is arranged to provide the first and second null control signals such that offset voltages associated with each of the first and second amplifiers means are selectively zeroed in response to the respective one of the first and second null control signals.

16. The apparatus of Claim 15, wherein the null control means comprises at least one of a shift register, a barrel shifter, a counter, an oscillator, a randomizer, and a power-on-reset circuit.

17. The apparatus of Claim 15, wherein the null control means is further arranged to activate one of the first and second null control signals at a time.

18. The apparatus of Claim 15, further comprising a third amplifier means that includes a third output that is coupled to the common node, a third input that is arranged to receive the feedback signal, and a third null control input that is arranged to receive a third null control signal, wherein the null control means is further arranged to provide the third control signal such that the offset voltage associated with each of the first, second, and third amplifier means are selectively zeroed in response to the respective one of the first, second, and third null control signals.

19. The apparatus of Claim 18, wherein the null control means is further arranged to assert one of the first, second, and third null control signals when the others of the first, second, and third null control signals are deasserted.

20. A method for reducing the offset voltage associated with a reference signal, comprising:

coupling together the outputs from an array of amplifier circuits at a common node to provide an intermediate signal;

coupling the common node to a second stage circuit;

generating the reference signal as an output of the second stage circuit that is responsive to the intermediate signal;

providing a feedback signal to the array of amplifier circuits in response to the reference signal;

selecting one of the array of amplifier circuits;

nulling an offset voltage associated with the selected amplifier circuit while the selected amplifier circuit is offline; and

maintaining the non-selected amplifier circuits such that the offset voltage associated with the reference signal is zeroed as an average.